AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit (IC) device, comprising:

a first bus interface unit to send a transaction packet over a first bus and not a second bus;

a second bus interface unit to send a transaction packet over ~~a~~ the second bus and not the first bus; and

a queue to store information that characterizes a plurality of bus transactions to be claimed by one of the first and second bus interface units and performed over one of the first and second buses,

wherein the IC device can be configured to operate in a first way that does not give either bus interface unit preference over the other when claiming a transaction from the queue,

and wherein the IC device can be configured to operate in a second way in which the first bus interface unit is preferred over the second bus interface unit when claiming a transaction from the queue.

2. (Original) The IC device of claim 1 wherein the queue is to store information that characterizes the plurality of transactions as split transactions,

and wherein each transaction is to be performed in the second way by the first bus interface unit sending a request packet for said transaction over the first bus and not the second bus, and the second bus interface unit receiving a completion packet for said transaction over the second bus and not the first bus.

3. (Original) The IC device of claim 1 further comprising:

a third bus interface unit to send a transaction packet over a third bus and not the first bus and not the second bus,

and wherein the IC device can be configured to operate in the second way so that the second bus interface unit is preferred over the third bus interface unit when claiming said transaction from the queue.

4. (Currently Amended) An integrated circuit (IC) device, comprising:

a first bus interface unit to send transaction information over a first bus and not a second bus, the first bus interface unit having a bus arbiter and a send block;

a second bus interface unit to send transaction information over ~~a~~ the second bus and not the first bus; and

a queue to store information that characterizes a plurality of bus transactions to be claimed by one of the first and second bus interface units for being performed over one of the first and second buses,

wherein the send block is to a) monitor the queue for transactions that are ready to be performed, b) request the first bus through the arbiter, and c) format and send a transaction packet into the first bus,

wherein the arbiter gives preference to the send block over other bus agents in response to a preference signal being asserted.

5. (Currently Amended) The IC device of claim 4 wherein the first bus interface unit further comprises a receive block to decode transaction packets received over the first bus, in response to being activated by the arbiter.

6. (Currently Amended) The IC device of claim 4 wherein the send block further includes a software-programmable timer that is to be set to a predetermined value each time the send block obtains ownership of the first bus, to prevent a non-preferred agent from holding the first bus ~~too long~~.

7. (Original) The IC device of claim 4 wherein the send block further includes means for balancing bandwidth on the first bus with latency associated with transactions on the first bus.

8. (Currently Amended) An integrated circuit (IC) device, comprising:

a first bus interface unit to send a transaction packet over a first bus and not a second bus;

a second bus interface unit to send a transaction packet over ~~a~~ the second bus and not the first bus; and

a queue to store information that characterizes a plurality of bus transactions to be claimed by one of the first and second bus interface units for being performed over one of the first and second buses,

wherein to prevent the same transaction from being sent over two buses simultaneously, one of the first and second bus interface units, which is preferred over the other, is to block the other when claiming a transaction from the queue.

9. (Original) The IC device of claim 8 being programmable by software to allow the first and second bus interface units to be configured for one of a) bi-directional bus operation for each, and b) bi-directional operation for both where each has a dominant direction of packet travel that is opposite to the other.

10. (Original) The IC device of claim 7 wherein request packets, for a plurality of claimed transactions, respectively, are to be sent predominantly by the first bus interface unit rather than the second bus interface unit, and completion packets, for said plurality of claimed transactions, respectively, are to be received predominantly by the second bus interface unit rather than the first bus interface unit.

11. (New) A method for performing bus transactions using multiple buses, comprising:

sending a transaction packet over a first bus and not a second bus, using a first bus interface;

sending a transaction packet over the second bus and not the first bus, using a second bus interface;

buffering information that characterizes a plurality of bus transactions to be claimed by one of the first and second bus interfaces to be performed over one of the first and second buses;

operating the bus interfaces in a first way that does not give either bus interface preference over the other when claiming a buffered transaction; and

operating the bus interfaces in a second way in which the first bus interface is preferred over the second bus interface when claiming a buffered transaction.

12. (New) The method of claim 11 wherein the buffered transactions are split transactions, the method further comprising:

while operating in the second way, sending a request packet for a transaction over the first and not the second bus using the first bus interface; and

receiving a completion packet for the transaction over the second bus and not the first bus, by the second bus interface.

13. (New) The method of claim 11 further comprising:

sending a transaction packet over a third bus and not the first bus and not the second bus, using a third bus interface; and

operating in the second way so that the second bus interface is preferred over the third bus interface when claiming the buffered transaction.